

Instruction templates

16-bit instruction template

op_16	15	7	6	2	1	0
	$operand_{[8:0]}$			$opcode_{[4:0]}$	$sz_{[1:0]}$	

32-bit instruction template

op_32	15	7	6	2	1	0
	$operand_{[8:0]}$			$opcode_{[4:0]}$	$sz_{[1:0]}$	
	$operand_{[17:9]}$			$opcode_{[9:5]}$	$sz_{[3:2]}$	

64-bit instruction template

op_64	15	7	6	2	1	0
	$operand_{[8:0]}$			$opcode_{[4:0]}$	$sz_{[1:0]}$	
	$operand_{[17:9]}$			$opcode_{[9:5]}$	$sz_{[3:2]}$	
	$operand_{[26:18]}$			$opcode_{[14:10]}$	$sz_{[5:4]}$	
	$operand_{[35:27]}$			$opcode_{[19:15]}$	$sz_{[7:6]}$	

128-bit instruction template

op_128	15	7	6	2	1	0
	$operand_{[8:0]}$			$opcode_{[4:0]}$	$sz_{[1:0]}$	
	$operand_{[17:9]}$			$opcode_{[9:5]}$	$sz_{[3:2]}$	
	$operand_{[26:18]}$			$opcode_{[14:10]}$	$sz_{[5:4]}$	
	$operand_{[35:27]}$			$opcode_{[19:15]}$	$sz_{[7:6]}$	
	$operand_{[44:36]}$			$opcode_{[24:20]}$	$sz_{[9:8]}$	
	$operand_{[53:45]}$			$opcode_{[29:25]}$	$sz_{[11:10]}$	
	$operand_{[62:54]}$			$opcode_{[34:30]}$	$sz_{[13:12]}$	
	$operand_{[71:63]}$			$opcode_{[39:35]}$	$sz_{[15:14]}$	

16-bit instruction formats

one operand with immediate

oplri_16 # op ra, imm	15	13	12	7	6	2	1	0
	$ra_{[2:0]}$		$imm_{[5:0]}$			$opcode_{[4:0]}$	00	

two operand with immediate

	15	13	12	10	9	7	6	2	1	0
op2ri_16 # op ra, rb, imm	<i>ra</i> _[2:0]		<i>rb</i> _[2:0]		<i>imm</i> _[2:0]		<i>opcode</i> _[4:0]		00	

three operand

	15	13	12	10	9	7	6	2	1	0
op3r_16 # op ra, rb, rc	<i>ra</i> _[2:0]		<i>rb</i> _[2:0]		<i>rc</i> _[2:0]		<i>opcode</i> _[4:0]		00	

32-bit instruction formats

one operand with immediate

oplri_32 # op ra, imm	15	13	12	7	6	2	1	0
	$ra_{[2:0]}$		$imm_{[5:0]}$			$opcode_{[4:0]}$	01	
	$ra_{[5:3]}$		$imm_{[11:6]}$			$opcode_{[9:5]}$	11	

two operand with immediate

op2ri_32 # op ra, rb, imm	15	13	12	10	9	7	6	2	1	0
	$ra_{[2:0]}$		$rb_{[2:0]}$		$imm_{[2:0]}$		$opcode_{[4:0]}$		01	
	$ra_{[5:3]}$		$rb_{[5:3]}$		$imm_{[5:3]}$		$opcode_{[9:5]}$		11	

three operand

op3r_32 # op ra, rb, rc	15	13	12	10	9	7	6	2	1	0
	$rc_{[2:0]}$		$rb_{[2:0]}$		$ra_{[2:0]}$		$opcode_{[4:0]}$	01		
	$rc_{[5:3]}$		$rb_{[5:3]}$		$ra_{[5:3]}$		$opcode_{[9:5]}$	11		

64-bit instruction formats

one operand with immediate

op1ri_64 # op ra, imm

15	13	12	7	6	2	1	0
$ra_{[2:0]}$		$imm_{[5:0]}$			$opcode_{[4:0]}$		10
$ra_{[5:3]}$		$imm_{[11:6]}$			$opcode_{[9:5]}$		11
$ra_{[8:6]}$		$imm_{[17:12]}$			$opcode_{[14:10]}$		11
$ra_{[11:9]}$		$imm_{[23:18]}$			$opcode_{[19:15]}$		11

two operand with immediate

op2ri_64 # op ra, rb, imm

15	13	12	10	9	7	6	2	1	0
$ra_{[2:0]}$		$rb_{[2:0]}$		$imm_{[2:0]}$		$opcode_{[4:0]}$		10	
$ra_{[5:3]}$		$rb_{[5:3]}$		$imm_{[5:3]}$		$opcode_{[9:5]}$		11	
$ra_{[8:6]}$		$rb_{[8:6]}$		$imm_{[8:6]}$		$opcode_{[14:10]}$		11	
$ra_{[11:9]}$		$rb_{[11:9]}$		$imm_{[11:9]}$		$opcode_{[19:15]}$		11	

three operand

op3r_64 # op ra, rb, rc

15	13	12	10	9	7	6	2	1	0
$rc_{[2:0]}$		$rb_{[2:0]}$		$ra_{[2:0]}$		$opcode_{[4:0]}$		10	
$rc_{[5:3]}$		$rb_{[5:3]}$		$ra_{[5:3]}$		$opcode_{[9:5]}$		11	
$rc_{[8:6]}$		$rb_{[8:6]}$		$ra_{[8:6]}$		$opcode_{[14:10]}$		11	
$rc_{[11:9]}$		$rb_{[11:9]}$		$ra_{[11:9]}$		$opcode_{[19:15]}$		11	

128-bit instruction formats

one operand with immediate

op1ri_128 # op ra, imm

15	13	12	7	6	2	1	0
$ra_{[2:0]}$		$imm_{[5:0]}$			$opcode_{[4:0]}$		11
$ra_{[5:3]}$		$imm_{[11:6]}$			$opcode_{[9:5]}$		11
$ra_{[8:6]}$		$imm_{[17:12]}$			$opcode_{[14:10]}$		11
$ra_{[11:9]}$		$imm_{[23:18]}$			$opcode_{[19:15]}$		11
$ra_{[14:12]}$		$imm_{[29:24]}$			$opcode_{[24:20]}$		11
$ra_{[17:15]}$		$imm_{[35:30]}$			$opcode_{[29:25]}$		11
$ra_{[20:18]}$		$imm_{[41:36]}$			$opcode_{[34:30]}$		11
$ra_{[23:21]}$		$imm_{[47:42]}$			$opcode_{[39:35]}$		11

two operand with immediate

op2ri_128 # op ra, rb, imm

15	13	12	10	9	7	6	2	1	0
$ra_{[2:0]}$		$rb_{[2:0]}$		$imm_{[2:0]}$		$opcode_{[4:0]}$		11	
$ra_{[5:3]}$		$rb_{[5:3]}$		$imm_{[5:3]}$		$opcode_{[9:5]}$		11	
$ra_{[8:6]}$		$rb_{[8:6]}$		$imm_{[8:6]}$		$opcode_{[14:10]}$		11	
$ra_{[11:9]}$		$rb_{[11:9]}$		$imm_{[11:9]}$		$opcode_{[19:15]}$		11	
$ra_{[14:12]}$		$rb_{[14:12]}$		$imm_{[14:12]}$		$opcode_{[24:20]}$		11	
$ra_{[17:15]}$		$rb_{[17:15]}$		$imm_{[17:15]}$		$opcode_{[29:25]}$		11	
$ra_{[20:18]}$		$rb_{[20:18]}$		$imm_{[20:18]}$		$opcode_{[34:30]}$		11	
$ra_{[23:21]}$		$rb_{[23:21]}$		$imm_{[23:21]}$		$opcode_{[39:35]}$		11	

three operand

op3r_128 # op ra, rb, rc

15	13	12	10	9	7	6	2	1	0
$rc_{[2:0]}$		$rb_{[2:0]}$		$ra_{[2:0]}$		$opcode_{[4:0]}$		11	
$rc_{[5:3]}$		$rb_{[5:3]}$		$ra_{[5:3]}$		$opcode_{[9:5]}$		11	
$rc_{[8:6]}$		$rb_{[8:6]}$		$ra_{[8:6]}$		$opcode_{[14:10]}$		11	
$rc_{[11:9]}$		$rb_{[11:9]}$		$ra_{[11:9]}$		$opcode_{[19:15]}$		11	
$rc_{[14:12]}$		$rb_{[14:12]}$		$ra_{[14:12]}$		$opcode_{[24:20]}$		11	
$rc_{[17:15]}$		$rb_{[17:15]}$		$ra_{[17:15]}$		$opcode_{[29:25]}$		11	
$rc_{[20:18]}$		$rb_{[20:18]}$		$ra_{[20:18]}$		$opcode_{[34:30]}$		11	
$rc_{[23:21]}$		$rb_{[23:21]}$		$ra_{[23:21]}$		$opcode_{[39:35]}$		11	